In re Patent Application of:
ROCHE ET AL.
Serial No. **10/039,765**
Confirmation No. **9186**
Filed: **NOVEMBER 7, 2001**

REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application,

The independent claims have been amended for better readability in terms of 1) when the master device is sending data to the slave device and the slave device is receiving the data from the master device, and 2) when the slave device is sending data to the master device and the master device is receiving the data from the slave device. In addition, the

In addition, the independent claims have been amended to more clearly define over the prior art references. The master device releases the data on the data line after the clock line is released by the slave device and by the master device; and the slave device releases the data on the data line after the clock line is released by the master device and the slave device.

Independent Claim 32 and its dependent claims have been cancelled. The claim amendments and arguments supporting patentability of the claims are provided below.

I. The Claimed Invention

The present invention, as recited in amended independent Claim 20, for example, is directed to a method of transmitting data between a master device and a slave device via a clock line and at least one data line, with the clock line being maintained by default on a first logic value. Each master

and slave device is able to tie the clock line to a potential representing a second logic value opposite the first logic value. The method comprises:

when the master device is sending data to the slave device and the slave device is receiving the data from the master device, then

the master device applies data to the data line, then ties the clock line to the second logic value,

the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data,

the slave device maintains the tie to the clock line at the second logic value while the slave device has not read the data,

the slave releases the tie to the clock line at the second logic value when the slave device has read the data, and

the master device maintains the data on the data line at least until an instant when the clock line is released by the slave device,

the master device releases the data on the data line after the clock line is released by the slave device and by the master device; and

when the slave device is sending data to the master device and the master device is receiving the data from the

slave device, then

the master device ties the clock line to the second logic value,

the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and then or simultaneously applies the data to the data line,

the master device maintains the tie to the clock line at the second logic value while the master device has not read the data,

the master device release the tie to the clock line at the second logic value when the master device has read the data,

the slave device maintains the data on the data line at least until an instant when the clock line is released by the master device, and

the slave device releases the data on the data line after the clock line is released by the master device and the slave device.

The present invention may advantageously provide a double control of the line by which each device - a master or a slave - can be considered as a master as far as the duration of the clock period is concerned. This advantageously allows each device to impose its operating speed on the other, particularly in the event of disparity of clock frequencies or when one of the devices operates in multitasking on applications that have

priority over the data transmission itself.

Independent Claim 48 is directed to a synchronous data transmission system, and has been amended similar to independent Claim 20.

II. The Claims Are Patentable

The Examiner rejected independent Claims 20 and 48 over the SPI Block Guide in view of the System Management Bus (SMBus) Specification.

The Examiner has taken the position that FIG. 4-2 on page 27 in the SPI Block Guide illustrates that the clock line is maintained by default on a first logic value (SCK=1), and that one of the devices has the ability to tie the clock line to a potential representing a second logic value opposite the first logic value (SCK=0 at SCK Edge No. 1). The Examiner also characterized the SPI Block Guide as disclosing that the clock line is tied to the second logic value, via the two devices, after data is applied to the data line (data is applied before SCK Edge No. 1), and data on the data line is maintained by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent (data is applied until rising edge of clock).

As correctly noted by the Examiner, the SPI Block Guide fails to disclose that the tie to the clock line is maintained by the device to which the data is sent while the device has not read the data. The Examiner cited the SMBus

Specification as disclosing this feature. In particular, the Examiner referenced FIG. 4-7 on page 22 in section 4.3.3.

The Examiner has taken the position that it would have been obvious to have the device receiving data to hold the clock down, as disclosed by the SMBus Specification, in the method disclosed by the SPI Block Guide since this would allow clock synchronization so that slower slave devices could interface with faster masters. The Applicants submit that even if the references were selectively combined as suggested by the Examiner, the claimed invention is still not provided.

The independent claims have been amended to more clearly define over the prior art references. For example, the master device releases the data on the data line after the clock line is released by the slave device and by the master device; and the slave device releases the data on the data line after the clock line is released by the master device and the slave device.

As noted above, the release of the clock line corresponds to a change from the second logic value to the first logic value only if the other device has already released the clock line. For example, reference is directed to FIGS. 3A, 3B in the Applicants' application where the sender (master device) can release the clock line before the receiver (slave device) or vice-versa. Reference is directed to FIGS. 5A, 5B we can note that in the Applicants' application where the sender (slave device) can release the clock line before the receiver (master

device) or vice-versa. In other words, when the sender is the first to release the clock line, the receiver continues to be tie the clock line. In this case, the sender must wait until the clock line returns to the first value before releasing the data.

Conversely, when the sender is the second to release the clock line, the clock line immediately returns to the first value. In this case, the sender is not obliged to continue to wait before releasing the data since it knows immediately that the receiver has already released the clock line. In effect, the device sending the data cannot know that the device to which the data is sent has released the clock line until it itself has released the clock line.

The Examiner has taken the position that the SPI Block Guide and SMBus Specification further disclose the master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the slave device (FIG. 4-2 in SPI Block Guide), the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device (Section 4.3.3, FIG. 4-7 in SMBus Specification), wherein the master device ties the clock line to the second logic value when the master device receives data from the slave device and wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies data to the data line when the slave

device is sending data to the master device (FIG. 4-2 in SPI Block Guide; Section 4.3.3, FIG. 4-7 in SMBus Specification).

The Applicants further submit that this feature of the claimed invention is not disclosed in the SPI Block Guide or in the SMBus Specification, even if the protocol is inverted. In effect, the SPI Block Guide discloses that the master ties the clock to a second value (FIG. 4-2) when the master device receives data from the slave device and fails to disclose that when the slave device detects the second logic value on the clock line, the slave device ties the clock line to the second logic value and applies data to the data line.

The SMBus Specification merely suggests that the slave device ties the clock line to the second logic value outside the period of data validity. Therefore, in a SMB bus, when the slave device is sending data to the master device, the slave device uses the possibility to stretch the clock by tying the clock line to the second value when it cannot send the data to the master device. The SPI Block Guide and the SMBus Specification, alone or in combination, fail to teach or suggest that the slave device ties the clock when it is sending data.

Futhermore, even if one skilled in the art were to "invert" the SMB protocol, the claimed invention is still not produced. "Inverting the protocol" is interpreted to mean that one skilled in the art would stretch the clock during the period of data validity and not outside the period of data validity. However, stretching the clock during the period of data validity

is not the only feature of the claimed invention. Assuming that the slave device is the device receiving the data and that the slave device stretches the clock, this does not imply that the master device maintains the data on the data line at least until an instant when the clock line is released by the slave device. This other feature is not suggested by the SMBis Specification. On the contrary, according to the SMBus Specification, an "inverted" would mean that the slave device would stretch the clock during the period of data validity after having read the data, to postpone the sending of new data, without the master device being obliged to maintain the data on the data line until the clock line is released by the slave device.

In other words, the SMBus Specification proposes to stretch the clock line only to postpone the sending of the further data, and does not propose to stretch the clock line to implement a handshaking technique by which the device which is receiving the data can say "It is OK I have read the data" to the device sending the data. According to the SMBus Specification "inverted" or "not inverted" stretching of the clock line is merely a means to prevent the clock from changing state, because such a changing if state prepare the next sending of data.

Accordingly, it is submitted that amended independent Claim 20 is patentable over the SPI Block Guide in view of the SMBus Specification. Amended independent Claim 48 is similar to

amended independent Claim 20. Therefore, it is submitted that this claim is also patentable over the the SPI Block Guide in view of the SMBus Specification.

In view of the patentability of amended independent Claims 20 and 48, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

III. CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

MICHAEL W. TAYLOR
Reg. No. 43,182
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330